**General Requirements (Tag prefix: RTC)**

Asynchronous, low active reset

1. The top-level input signal ‘reset\_n’ shall be mapped to the internal signal ‘i\_resetn’.
2. All modules shall be set to their initial values when ‘i\_reset\_n’ is 0.

Positive edge clocking

1. The top-level input signal ‘sys\_clk’ shall be mapped to the internal signal ‘i\_sclk’.
2. All synchronous operations shall be done on the positive edge of ‘sys\_clk’.

Active high trigger

1. The top-level input signal ‘trigger\_in’ shall be mapped to the internal signal ‘i\_trigger’.

**10 Millisecond Timer (Tag prefix: TIMER)**

**24-Bit BCD Up Counter (Tag prefix: COUNTER)**

4-bit counter submodule with asynchronous reset and parameterizable rollover value.

1. ‘o\_bcdcount’ shall be set to “0000” when ‘i\_resetn’ is 0.
2. ‘o\_bcdcount’ shall be reset to “0000” when ‘o\_bcdcount’ is equal to rollover\_count + 1.

Internal state machine driven by trigger detection signals.

1. All state transitions shall occur on the positive edge of ‘i\_rtcclk’.
2. Module shall be initialized in the idle state.
3. Module shall transition from idle state to count state when ‘i\_countenb’ and ‘i\_latchcount’ are set to 1.
4. Module shall transition from count state to idle state when ‘i\_latchcount’ is 0.]]
5. When in the idle state, ‘o\_bcdcount’ shall keep its current value.
6. When in the count state, ‘o\_bcdcount’ shall increment on the positive edge of ‘i\_rtcclk’.

Top level module sends the individual BCD digits to a single bus output.

1. The module shall instantiate six 4-bit counter submodules corresponding to each displayed digit.
2. ‘o\_count (3:0)’ shall be set to the corresponding bits from ‘o\_bcdcount0’.
3. ‘o\_count (7:4)’ shall be set to the corresponding bits from ‘o\_bcdcount1’.
4. ‘o\_count (11:8)’ shall be set to the corresponding bits from ‘o\_bcdcount2’.
5. ‘o\_count (15:12)’ shall be set to the corresponding bits from ‘o\_bcdcount3’.
6. ‘o\_count (19:16)’ shall be set to the corresponding bits from ‘o\_bcdcount4’.
7. ‘o\_count (23:20)’ shall be set to the corresponding bits from ‘o\_bcdcount5’.

**7-Segment Display**

**Traceability:**